ABSTRACT

The present invention provides integrated circuit fabrication methods and devices wherein triple damascene structures are formed in five consecutive dielectric layers (312, 314, 316, 318 and 320), using two etching sequences. A first etching sequence comprising: depositing a first etch mask layer (322), on the fifth (top) layer (320), developing a power line trench pattern (324) and a via pattern (326) in the first mask layer, simultaneously etching the power line trench pattern (324) and the via pattern (326) through the top three dielectric layers (316, 318, 320), and removing the first etch mask layer. A second etching sequence including: depositing a second etch mask layer (330), on the fifth layer (320) and inside the power line trench (325) formed in the first etching sequence, developing a signal line pattern (332) overlaying the via pattern (327) in the second etch layer, etching the via pattern (327) through the second layer (312), and subsequently etching the via pattern (327) through the first layer (312) while simultaneously etching the signal line trench pattern (332) through the fifth layer (320). The etching sequences result in the formation of a power line trench (325) and a signal line trench (336) with an underlying via hole (340). These trenches and the via hole are simultaneously filled with a conductive material, such as a metal, to form a triple damascene structure including a power line (352) and a signal line (354) having an underlying via plug (356). This triple damascene structure uses three design rules while only requiring two etch mask layers, and only one planarizing or etch back stop to define the interconnect lines. Similar novel techniques can be employed to fabricate a quadruple damascene structure including a power line (450) having an underlying via plug (452) and a signal line (454) with an underlying via plug (456), while using four design rules. The inventive techniques can also be utilized to form similar triple and quadruple damascene structures in a variety of dielectric stacks. In additional embodiments, manufacturing systems (1110) are provided for fabricating IC structures, such as the novel damascene structures. These systems include a controller (1100) which is adapted for interacting with a plurality of fabrication stations (1120, 1122, 1124, 1126, 1128, 1130 and 1132).